Code No: P18ECT09

HALL TICKET NUMBER

PACE INSTITUTE OF TECHNOLOGY & SCIENCES::ONGOLE
(AUTONOMOUS)
III B.TECH I SEMESTER END REGULAR EXAMINATIONS, DEC/JAN – 2022/23
LINEAR AND DIGITAL IC APPLICATIONS
(ECE Branch)

Time: 3 hours Max. Marks: 60

Note: Question Paper consists of Two parts (Part-A and Part-B)

PART-A

Answer all the questions in Part-A (5X2=10M)

Q. No.		Questions	Marks	CO	KL
1.	a)	Draw the circuit diagram of the basic current mirror.	[2M]	1	L1
	b)	Write the Op-Amp DC and AC Characteristics	[2M]	2	L1
	c)	Draw the frequency response characteristics of the band elimination	[2M]	3	L1
	d)	Define the terms: Linearity and settling time with respect to DAC	[2M]	4	L1
	e)	Give the syntax and structure of a package in VHDL.	[2M]	3	L1

PART-B

Answer One Question from each UNIT (5X10=50M)

Q. No.		Questions	Marks	CO	KL
		UNIT-I			
2.	a)	Draw the basic block diagram of op-amp and explain the operation of each block.	[5M]	1	L2
	b)	Describe the working of a practical differentiator circuit. Derive the expression for output voltage.	[5M]	1	L1
		OR			
3.	a)	Explain the differential amplifier circuit and obtain the expressions for common mode gain and differential mode gain.	[5M]	1	L2
	b)	An op-amp has a slew rate of 2V/μs. What is the maximum frequency of an output sinusoid of peak value 5V at which the distortion sets in due to the slew rate limitation?	[5M]	1	L3
		UNIT-II			
4.	a)	Design the 2nd order LPF and explain its operation in detail.	[5M]	2	L3
	b)	Derive frequency of oscillations by using triangular wave generator.	[5M]	2	L3
		OR			
5.	a)	Explain the operation of an astable multivibrator using a 555 timer. Derive the expression for on and off-state time *periods*.	[5M]	2	L2
	b)	Explain the principles of individual blocks of PLL with a neat sketch	[5M]	2	L2
		UNIT-III			
6.	a)	Draw and explain the operation of R-2R ladder DAC	[5M]	3	L2

	b)	With neat sketch explain the operation of successive approximation ADC with one example	[5M]	3	L2
		OR			
7.	a)	Draw the circuit of weighted resistor DAC and derive expression for output analog voltage Vo.	[5M]	3	L2
	b)	What would be the output voltage produced by a D/A converter whose output range is 0 to 10V with a binary number 10111100(for a 8 bit DAC)	[5M]	3	L3
		UNIT-IV			
8.	a)	Explain the CMOS steady state and dynamic electrical behavior	[5M]	4	L2
	b)	Explain the following elements of VHDL? i) Structural design elements ii) Dataflow design elements	[5M]	4	L2
		OR			
9.	a)	Explain about inertial delay and Transport delay models in VHDL with examples	[5M]	4	L2
	b)	Why place and route tools are used in VHDL draw the data flow diagram of place and route tools and explain.	[5M]	4	L3
		UNIT-V			
10.	a)	Write a data-flow style VHDL program for 4:1 MUX.	[5M]	5	L3
	b)	Write a VHDL code for Ring counter.	[5M]	5	L3
		OR			
11.	a)	Write a VHDL code for four-bit parallel adder/subtractor.	[5M]	5	L3
	b)	Explain the Design of Modulus N Synchronous Counters	[5M]	5	L2

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